CMP slurry optimization for advanced nodes

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As advanced device manufacturers identify needs for new and additional CMP steps, new slurry solutions can deliver exceptional planarization and defectivity within a stable CMP process.

Advanced logic and memory device nodes demand significantly greater performance from chemical mechanical planarization/polishing (CMP) processes. Due to the fast growing number and increased diversity of non-metal CMP steps, new requirements are emerging, such as enhanced planarization efficiency, near-zero level defectivity and substantial reductions in process cost versus previous device nodes. Highly tunable and dilutable CMP slurries, in conjunction with matched CMP pads and processes are needed to achieve both technical and economic objectives. In advanced front-end-of-line (FEOL) processing, a variety of new CMP steps for different layer combinations, such as oxide, nitride and polysilicon, need to be polished and each layer requires different rates, selectivities and tight process control.

These varied requirements necessitate new slurry formulations. A new family of dielectric CMP slurries will be examined, which uses state-of-the-art colloidal silica abrasives paired with advanced additives to offer high removal rates, planarization efficiency and exceptionally low defect levels. These newly commercialized slurries are offered to customers in concentrate form to minimize overall cost-of-ownership (CoO). Point-of-use dilution minimizes abrasive concentration without sacrificing CMP performance and process stability.

CMP technical trends and challenges

The semiconductor industry continues to see growth in both logic and memory chip demand, driven by expanding applications in segments such as mobile, server, data processing, communications, consumer electronics, industrial and automotive. Scaling and cost reduction to extend Moore’s Law continue to drive the needs for new transistor/device architectures and technologies like 3D FinFETs, 3D NANDs and 3D packaging. CMP is a critical enabler to deliver these technologies.

In advanced logic nodes, there are an increased number of CMP layers (e.g., 22-28 layers at 7nm compared to 12 layers...
for 45nm). New technologies and material layers have not only offered additional opportunities but also presented new challenges for CMP consumables and tool sets [1].

In addition to low defectivity and reduced cost-of-ownership, key performance drivers such as planarization efficiency (PE), erosion, and dishing must have tight process control with-in-die (WID) and with-in-wafer (WIW) uniformity. New innovations are needed for these emerging requirements.

In advanced logic processes, the Polysilicon Open Polish (POP) requires nitride and oxide removal to then stop on polysilicon [2]. There is a need for a tunable slurry and stable pad life to enable low gate height variation and dishing. Self-Aligned Contacts (SAC) processes require polishing nitride and stopping on oxide; this necessitates use of a highly-selective slurry (nitride: oxide selectivity > 50:1). Multiple buff steps may be needed to generate nitride residual free surfaces, making a tunable slurry a good solution. Polysilicon gate CMP polishes amorphous- or polysilicon and stops in the same film. Gate height variation across the wafer is critical. Managing final thickness requirements through end-pointing is very challenging; preferably, it requires a pad/slurry process with some level of self-stopping and with high planarization efficiency for gate height control and low surface roughness. With shallow trench isolation (STI), since the needle-like structure fins are getting thinner and taller, there is a need for slurry with extremely high selectivity (>100:1 Ox: SiN) to minimize the nitride loss. New flowable CVD (FCVD) films used for gap-fill (e.g., in STI processes) are sensitive to deposition and annealing, and could cause high defectivity (particles) and rate instability.

Advanced memory applications are also incorporating additional CMP process steps (e.g., buff steps may be performed in a one-platen process with hard pads for improved defectivity and global uniformity after an etch step). There are enormous technical challenges to enable further scaling of current DRAM cell size. With the need for additional CMP steps, DRAM processes continue to demand higher removal rates to enable greater throughput and reduce overall CoO.

For advanced nodes, one consistency is that there are additional new CMP steps for both logic and memory (primarily 3D-NAND). Slurries with significant, characterized tunability, enabling low defectivity and a lower CoO, are required for multiple applications.

**New slurry formulations**

Semiconductor manufacturers rely on strong collaboration with materials suppliers to identify or develop slurries that meet these new specific and stringent requirements. As an example, Dow has recently developed slurry options that address higher oxide removal, lower defectivity and lower cost-of-ownership in both ≤ 20nm DRAM and ≤ 28nm logic applications. For ≤ 14nm logic applications, different process requirements warranted an oxide slurry with high planarization efficiency and step height reduction combined with good polysilicon and nitride removal rates.

One of the commercial slurry products developed as a result of these requests is Dow’s OPTIPLANE™ 2118 slurry, a low-abrasive, acidic pH silica slurry used for planarizing dielectric films in advanced CMP nodes. The enhanced CMP efficiency of this slurry is primarily enabled by a unique formulation that promotes favorable particle/wafer interaction. As demonstrated in the plot of zeta potential vs. pH (FIGURE 1), colloidal silica abrasives have the same negatively-charged surface as the polished TEOS films (throughout all measured pH ranges from pH 2 to pH 11) and thus exhibit undesirable electrostatic repulsion during polishing. With the introduction of proprietary additives in the formulation, the new slurry formulation possesses a significantly shifted isoelectric point (IEP) and creates a positively-charged surface at acidic pH via additive adsorption onto the silica particle surface. Under such conditions, the particles are intuitively attracted to the wafer surface such that the point-of-use (POU) abrasives can be significantly reduced without sacrificing removal rate performance (FIGURE 2). This optimized formulation reflects precise control.

![FIGURE 2. Silica abrasive-wafer interactions (a) without a charge modifying additive and (b) with a charge modifying additive.](image-url)
of the particle-wafer interface in order to maximize the CMP benefit.

The slurry consists of spherical colloidal silica particles and a proprietary additive which adsorbs onto the abrasive particles and reverses the charge from negative to positive as illustrated in Fig. 2. The resulting electrostatic attractive forces between the abrasive particles (+ve) and dielectric film (-ve) leads to increased polishing efficiency (material removal rate/abrasive loading) as shown in FIGURE 3. For commercially available alkaline colloidal and fumed silica slurries, achieving high dielectric removal rates at low abrasive loading is extremely challenging, and hence they are generally used at >12 wt. % abrasive content for typical ILD applications. In comparison, this new slurry formulation can be used at 6 wt. % abrasive content at point of use (POU) for such applications.

A variety of defects are generated during oxide CMP processes, including scratches, particle residues, pad debris and roughness-related non-visible defects. Scratches are widely believed to be the most detrimental to wafer yields. The onset of scratch formation is often a result of an increased number of large particles in the polishing slurry.²

OPTIPLANE 2118 has been formulated with highly controlled spherical silica particles and produced with advanced filtration technology. This slurry exhibited ~45% scratch reduction when used on undoped silica glass (USG) wafers (FIGURE 4) and demonstrates >70% scratch reduction on internal TEOS wafers compared to those polished with conventional fumed silica slurry under similar polishing processes. Such defect benefits, together with remarkably reduced pad wearing and polishing temperature, can be attributed to the use of low POU abrasive content and steric protection from additive adsorption on the polished surface.

While this new commercial slurry formulation is for dielectric applications, R&D teams are also developing and characterizing slurries with specific selectivities targeted at advanced FEOL CMP steps such as POP and SAC amongst others. Through internal development work and customer engagements, a wide range of rates and selectivities can be obtained from other formulations that will be commercialized in the OPTIPLANE 4000 series family.
Conclusion
As advanced device manufacturers identify needs for new and additional CMP steps, new slurry solutions can deliver exceptional planarization and defectivity within a stable CMP process. Advanced performance can be achieved while lowering process costs, through low point-of-use abrasive concentration, high removal rates and exceptional process consumable lifetime. New innovations in CMP slurries are helping to enable success at advanced nodes for next-generation manufacturing as the industry continues to move forward.

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References

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